CLAIMS

What is claimed is:

1. A method for testing cache performance of a processor design, the method comprising:

searching a file that contains test results for a lot of wafers; and

identifying at least one processor on one of the wafers in the lot in which a cache array has passed a cache test.

2. The method of claim 1, wherein the identifying the at least one processor comprises identifying that a built-in-self-test (BIST) engine in the at least one processor was able to execute the cache test.

3. The method of claim 1, further comprising identifying all of the processors in the lot in which a cache array has passed the cache test.

4. The method of claim 3, wherein the identifying all of the processors comprises identifying that a built-in-self-test (BIST) engine in each of the processors was able to execute the cache test.

5. The method of claim 1, wherein the searching the file comprises parsing the file.

6. The method of claim 1, wherein the searching the file comprises opening the file and parsing the file.

7. The method of claim 1, wherein the searching the file comprises decompressing the file.

8. A system for testing cache performance of a processor design, the system comprising:

a parser module for searching a file that contains test results for a lot of wafers; and

a cache-testable processor identification module for identifying processors on wafers in the lot in which a cache array has passed a cache test.

9. The system of claim 8, wherein the parser module is configured to open the file that contains the test results.

10. The system of claim 8, wherein the parser module and the cache-testable processor identification module comprise software that is executed by a processor.

11. The system of claim 8, wherein the cache-testable processor identification module is configured to identify the processors for which a built-in-self-test (BIST) engine was able to execute the cache test.

12. The system of claim 8, wherein the parser module and the cache-testable processor identification module comprise a PERL script.

13. A computer program embodied in a computer-readable medium, the program comprising:

logic configured to search a file that contains test results for a lot of wafers; and

logic configured to identify at least one processor on one of the wafers in the lot in which a cache array has passed a cache test.

14. The computer program of claim 13, wherein the logic configured to identify the at least one processor comprises logic configured to identify that a built-in-self-test (BIST) engine in the at least one processor was able to execute the cache test.

15. The computer program of claim 13, wherein the logic configured to search the file comprises logic configured to parse the file.

16. The computer program of claim 13, wherein the logic configured to search the file comprises logic configured to decompress the file.

17. A system for testing cache performance of a processor design, the system comprising:

means for searching a file that contains test results for a lot of wafers; and

means for identifying all processors on wafers in the lot in which a cache array has passed a cache test.